What is claimed is:

1. A test circuit for identification of locations with low speed performance comprising:

a grid of units, each unit having a first and second inverter, and the first and second inverter of each unit in a last column being coupled to each other;

first switches, each coupled between the first and second inverter of one of the units;

second switches, each coupled between the second and first inverter respectively of two adjacent units in a same column;

third switches, each coupled between the two first or second inverters of adjacent units in a same row;

pairs of serially connected fourth switch and third inverter, each coupled between the first and second inverter of one of the units in a first column; and

pairs of serially connected fifth switch and fourth inverter, each coupled between the second and first inverter respectively of a last and first unit in a same column.

2. The test circuit as claimed in claim 1, wherein the locations with low speed performance are identified according to frequencies of oscillation signals generated by rows of ring oscillators formed by opening the first, second and fifth switches, and closing the third and fourth switches, and columns of ring oscillators formed by closing

the first, second and fifth switches, and opening the third and fourth switches.

3. The test circuit as claimed in claim 1, wherein the first and second inverters are inverter strings having the same number of inverters.

4. The test circuit as claimed in claim 1, wherein the first and second inverter of one of the units are inverter strings comprising an even number of inverters.

5. A test circuit for identification of locations with low speed performance comprising:

a grid of units, each unit having a first and second inverter, and the first and second inverter of each unit in a last column being coupled to each other;

first transistors, each having a drain and source respectively coupled to the first inverter and the second inverter of one of the units;

second transistors, each having a drain and source respectively coupled to the second and first inverter of two adjacent units in a same column;

third transistors, each having a drain and source respectively coupled to the two first or second inverters of adjacent units in a same row;

pairs of serially connected fourth transistor and third inverter, each coupled between the first and second inverter of one of the units in a first column; and

pairs of serially connected fifth transistor and fourth inverter, each coupled between the second and first inverter of a last and first unit in a same column; and

a switch control circuit generating gate signals to gates of all the transistors.

6 The test circuit as claimed in claim 5, wherein the locations with low speed performance are identified according to frequencies of oscillation signals generated by rows of ring oscillators formed by the switch control circuit turning off the first, second and fifth transistors, and turning on the third and fourth transistors, and columns of ring oscillators formed by the switch control circuit turning on the first, second and fifth transistors, and turning off the third and fourth transistors.

7. The test circuit as claimed in claim 5, wherein the first and second inverters are inverter strings having the same number of inverters.

8. The test circuit as claimed in claim 5, wherein the first and second inverters of one of the units are inverter strings having an even number of inverters.

9. The test circuit as claimed in claim 5, wherein the gates of the third transistors are coupled to receive a control signal and the switch control circuit comprises:

a string of fifth inverters receiving the control signal, each of which has an input and output

terminal respectively coupled to the gates of the adjacent fourth and second transistors;

a sixth inverter has an input and output terminal respectively coupled to the gates of the adjacent fourth and fifth transistors; and

a seventh inverter has an output terminal coupled to all the gates of the first and second transistors, and an input terminal coupled to receive the control signal.

10. A test circuit for identification of defect locations resulting in low speed performance comprising:

a grid ring oscillator capable of detecting a propagation delay through vertical and horizontal branch circuits; and

circuitry for evaluating test results of both the vertical and horizontal branch circuits to identify critical locations with low speed performance.

11 The test circuit as claimed in claim 10, wherein the grid ring oscillator comprises:

a grid of units, each unit having a first and second inverter, and the first and second inverter of each unit in a last column being coupled to each other;

first switches, each coupled between the first and second inverter of one of the units;

second switches, each coupled between the second and first inverter respectively of two adjacent units in a same column;

third switches, each coupled between the two first or second inverters of adjacent units in a same row;

pairs of serially connected fourth switch and third inverter, each coupled between the first and second inverter of one of the units in a first column; and

pairs of serially connected fifth switch and fourth inverter, each coupled between the second and first inverter respectively of a last and first unit in a same column.

12. The test circuit as claimed in claim 11, wherein the locations with low speed performance are identified according to frequencies of oscillation signals generated by rows of ring oscillators formed by opening the first, second and fifth switches, and closing the third and fourth switches, and columns of ring oscillators formed by closing the first, second and fifth switches, and opening the third and fourth switches.

13. The test circuit as claimed in claim 11, wherein the first and second inverters are inverter strings having the same number of inverters.

14. The test circuit as claimed in claim 11, wherein the first and second inverter of one of the units are inverter strings comprising an even number of inverters.

15. The test circuit as claimed in claim 10, wherein the grid ring oscillator comprises:

a grid of units, each unit having a first and second inverter, and the first and second inverter of each unit in a last column being coupled to each other;

first transistors, each having a drain and source respectively coupled to the first inverter and the second inverter of one of the units;

second transistors, each having a drain and source respectively coupled to the second and first inverter of two adjacent units in a same column;

third transistors, each having a drain and source respectively coupled to the two first or second inverters of adjacent units in a same row;

pairs of serially connected fourth transistor and third inverter, each coupled between the first and second inverter of one of the units in a first column; and

pairs of serially connected fifth transistor and fourth inverter, each coupled between the second and first inverter of a last and first unit in a same column; and

a switch control circuit generating gate signals to gates of all the transistors.

16 The test circuit as claimed in claim 15, wherein the locations with low speed performance are identified according to frequencies of oscillation signals generated by

rows of ring oscillators formed by the switch control circuit turning off the first, second and fifth transistors, and turning on the third and fourth transistors, and columns of ring oscillators formed by the switch control circuit turning on the first, second and fifth transistors, and turning off the third and fourth transistors.

17. The test circuit as claimed in claim 15, wherein the first and second inverters are inverter strings having the same number of inverters.

18. The test circuit as claimed in claim 15, wherein the first and second inverters of one of the units are inverter strings having an even number of inverters.

19. The test circuit as claimed in claim 15, wherein the gates of the third transistors are coupled to receive a control signal and the switch control circuit comprises:

a string of fifth inverters receiving the control signal, each of which has an input and output terminal respectively coupled to the gates of the adjacent fourth and second transistors;

a sixth inverter has an input and output terminal respectively coupled to the gates of the adjacent fourth and fifth transistors; and

a seventh inverter has an output terminal coupled to all the gates of the first and second transistors, and an input terminal coupled to receive the control signal.